scan-path interface circuit, which allows for a readout of the storage contents of a prescribed memory or a register within the system through the [aforementioned] processor by the scan-path method; a switching circuit, which can be accessed by the [aforementioned] processor, and selectively switches the [aforementioned] scan-path interface circuit between [the] an enabled state and [the] a disabled state according to the prescribed switch control information given by the [aforementioned] processor; and a program storage means, which stores the program for the [aforementioned] processor to enable processing to give the [aforementioned] switch control information to the [aforementioned] switching circuit.

2. (Amended) Computer system described in Claim 1, [characterized by the aforementioned] wherein the switching circuit [having:] includes a register for holding the [aforementioned] switch control information which can be accessed by the [aforementioned] processor; and a gate circuit, [which is provided] in a signal path that is [connected] coupled to the [aforementioned] scan-path interface circuit and has an open state or a closed state according to the contents of the [aforementioned] register.

3. (Amended) Computer system described in Claim 1 [characterized by the [aforementioned]] wherein the switching circuit [having: a number of] includes password registers for holding the [aforementioned] switch control information which can be individually accessed by the [aforementioned] processor; a comparison means, which compares the contents of the number of [aforementioned] password registers with each other and which yields comparison results; and a gate circuit, [which is provided] in the signal path which is [connected] coupled to the [aforementioned] scan-path interface circuit, and has an open state or a closed state according to the comparison results from the [aforementioned] comparison means.